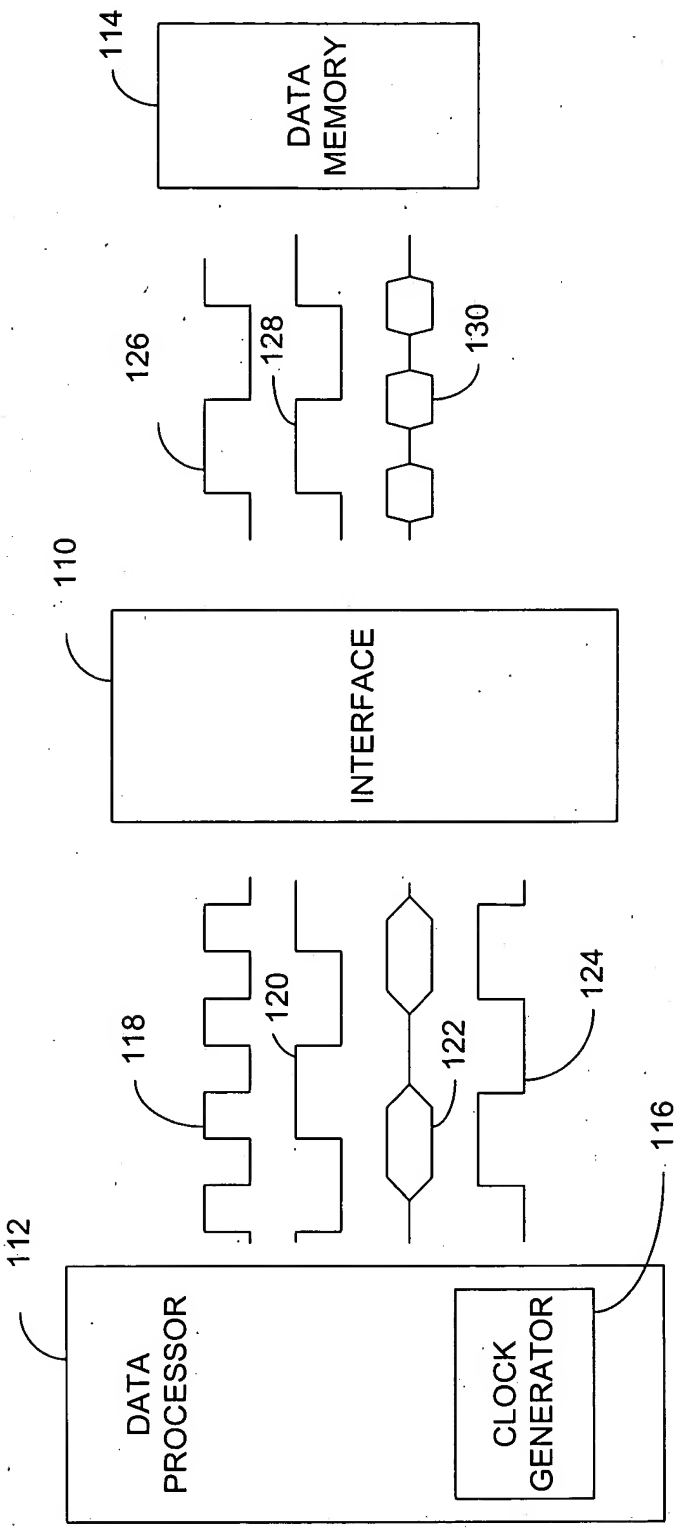
DATA PROCESSOR
CLOCK GENERATOR
INTERFACE
DATA MEMORY
112
110
114
116
118
120
122
124
126
128
130

FIG. 1

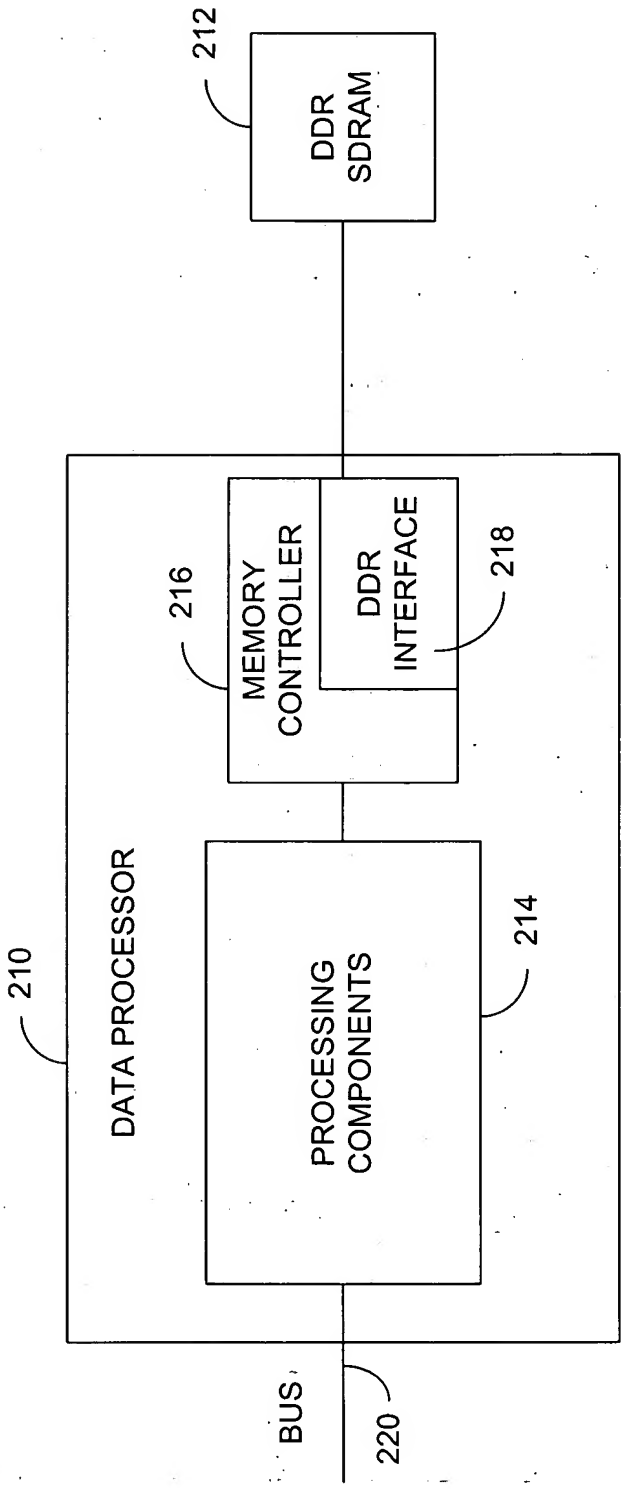
212
DDR SDRAM
DATA PROCESSOR
210
MEMORY CONTROLLER
216
DDR INTERFACE
218
PROCESSING COMPONENTS
214
BUS
220

FIG. 2

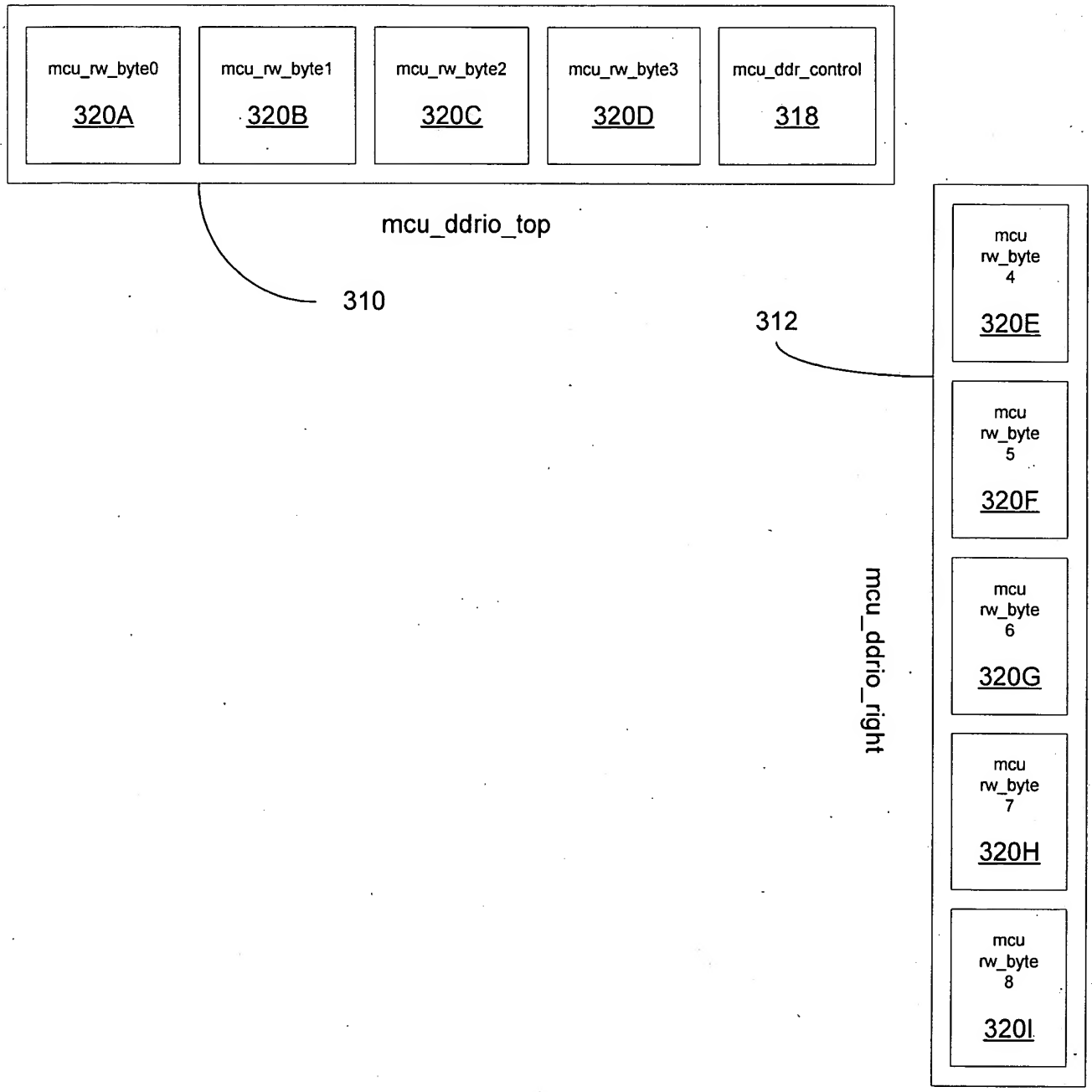
mcu_rw_byte0
320A
mcu_rw_byte1
320B
mcu_rw_byte2
320C
mcu_rw_byte3
320D
mcu_ddr_control
318
mcu_ddrio_top
310
312
mcu rw_byte 4
320E
mcu rw_byte 5
320F
mcu rw_byte 6
320G
mcu rw_byte 7
320H
mcu rw_byte 8
320I
mcu_ddrio_right

FIG. 3

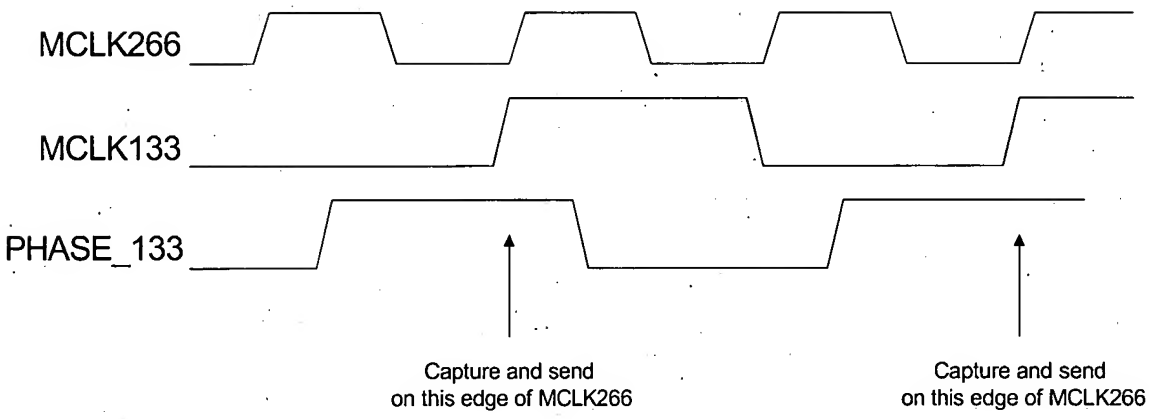
MCLK266
MCLK133
PHASE_133
Capture and send on this edge of MCLK266
Capture and send on this edge of MCLK266

FIG. 4

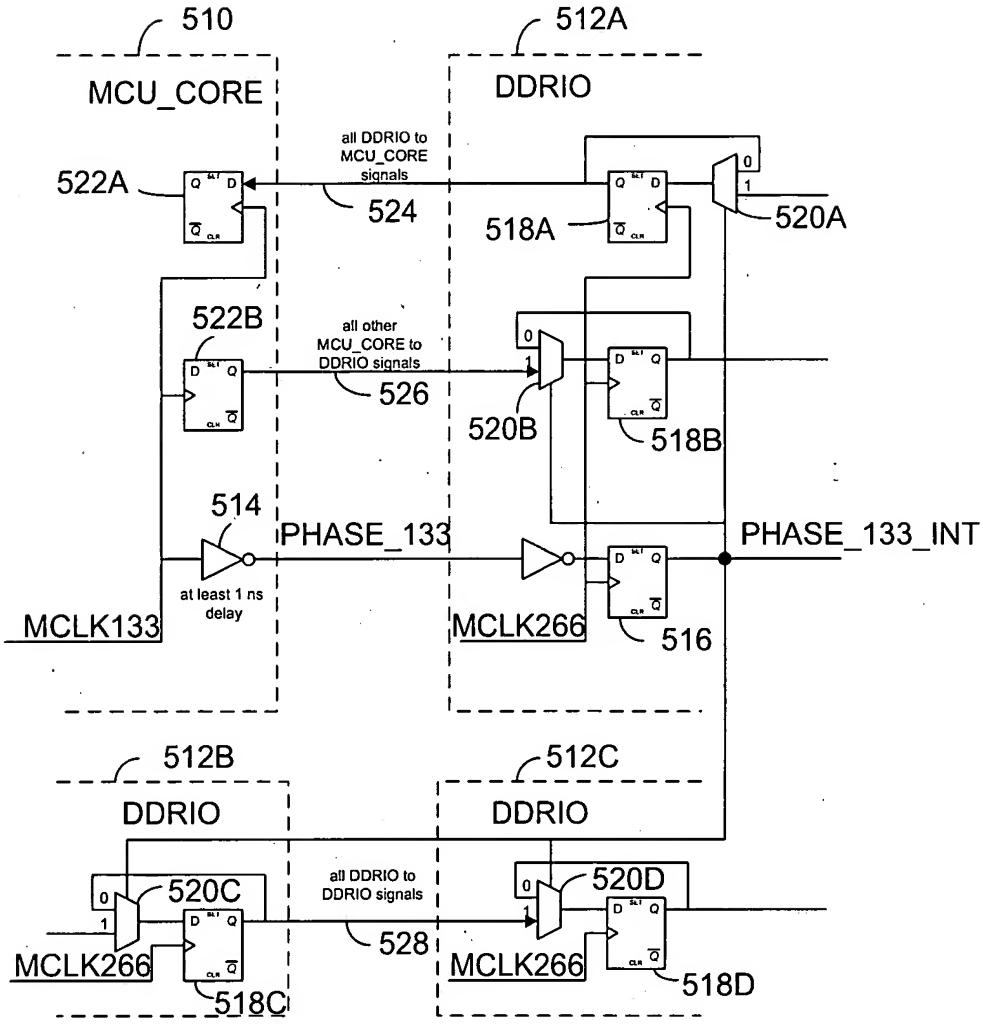
510
MCU_CORE
512A
DDRIO
all DDRIO to MCU_CORE signals
524
522A
518A
520A
522B
all other MCU_CORE to DDRIO signals
526
520B
518B
514
PHASE_133
PHASE_133_INT
at least 1 ns delay
MCLK133
MCLK266
516
512B
DDRIO
512C
DDRIO
all DDRIO to DDRIO signals
520C
520D
528
MCLK266
MCLK266
518C
518D

FIG. 5

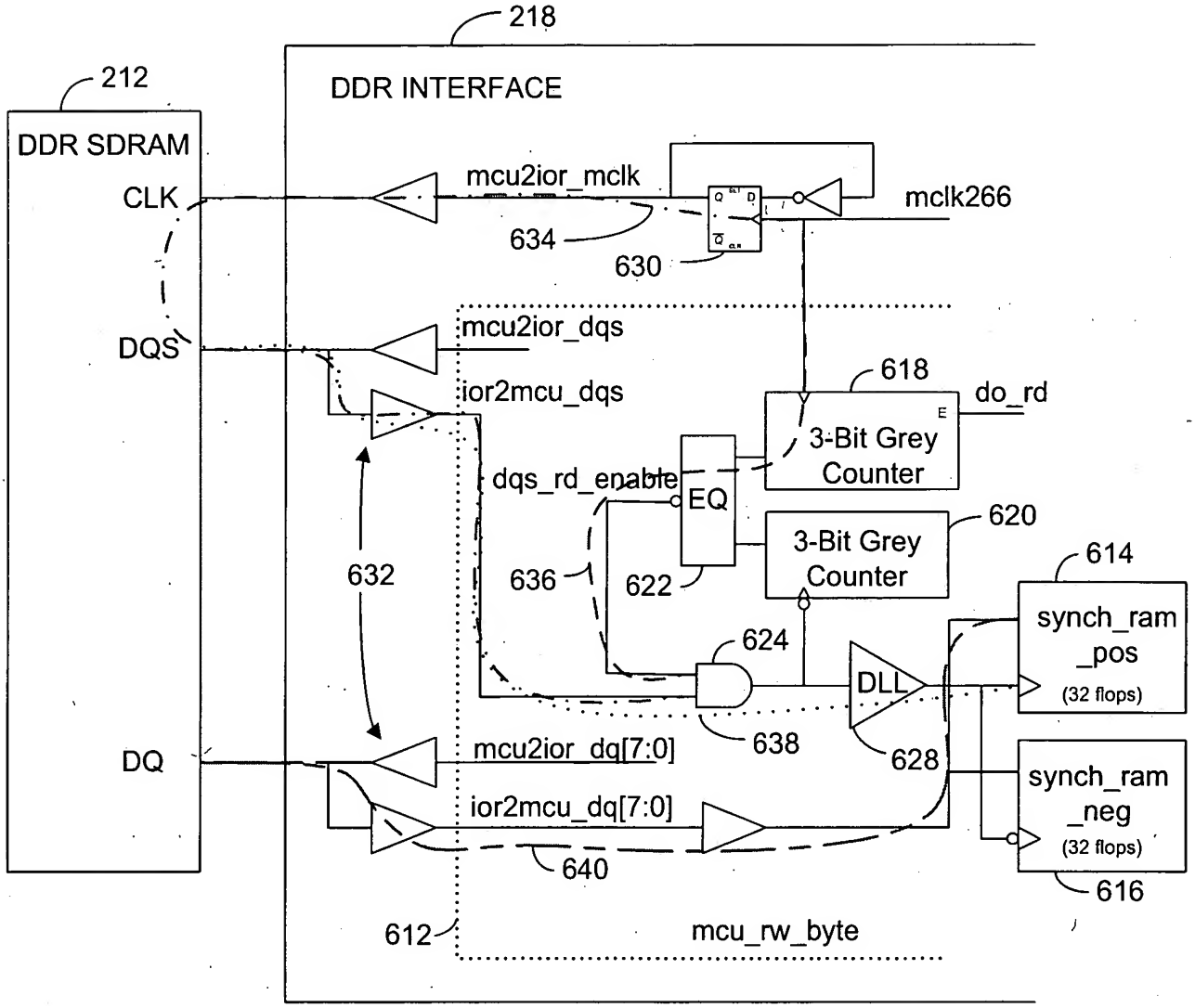
218
212
DDR INTERFACE
DDR SDRAM
CLK
DQS
DQ
mcu2ior_mclk
mclk266
634
630
mcu2ior_dqs
ior2mcu_dqs
618
do_rd
3-Bit Grey Counter
dqs_rd_enable
EQ
620
3-Bit Grey Counter
614
632
636
622
624
DLL
synch_ram _pos
(32 flops)
638
628
mcu2ior_dq[7:0]
ior2mcu_dq[7:0]
synch_ram _neg
(32 flops)
640
616
612
mcu_rw_byte

FIG. 6

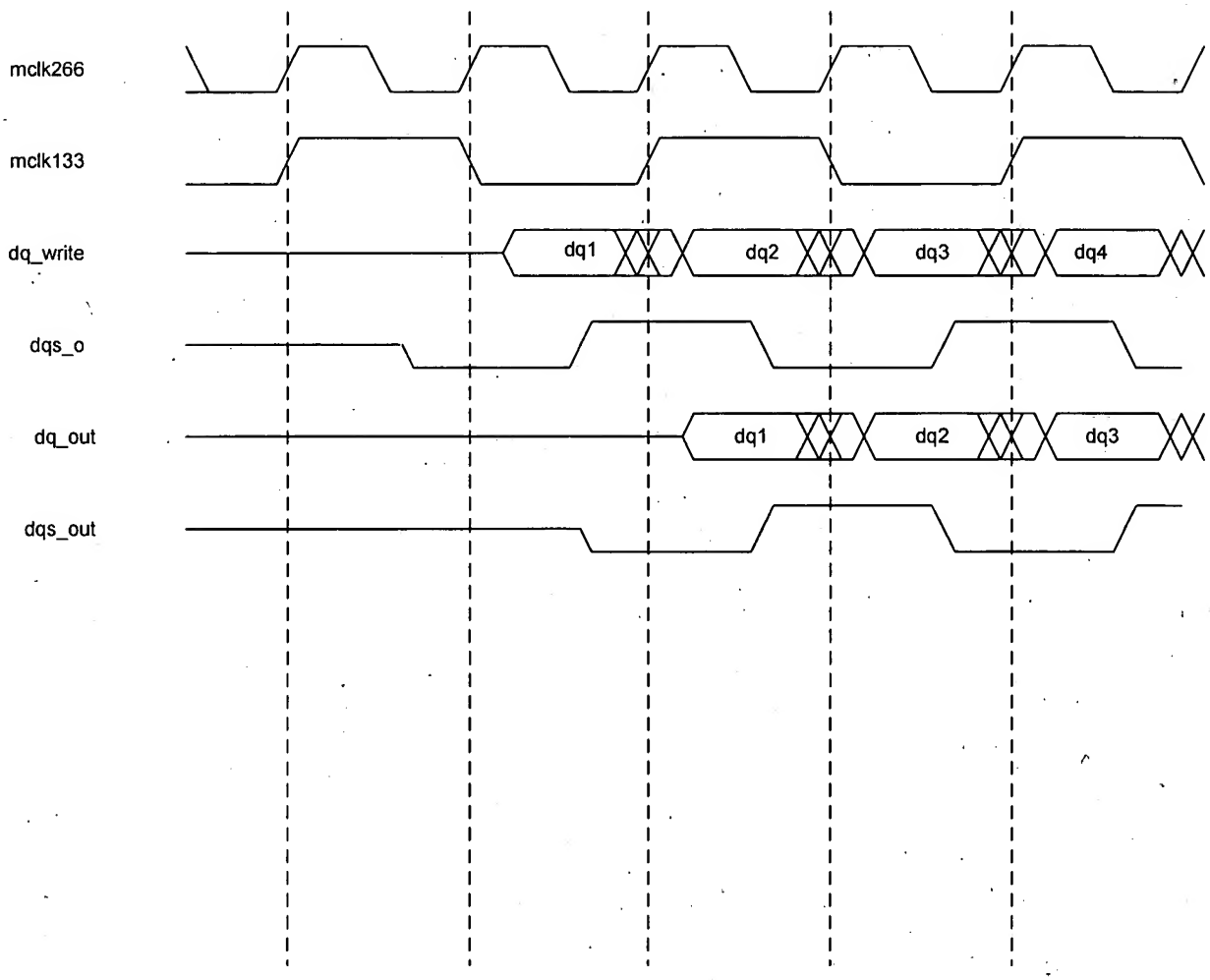
mclk266
mclk133
dq_write
dq1
dq2
dq3
dq4
dqs_o
dq_out
dq1
dq2
dq3
dqs_out

FIG. 7

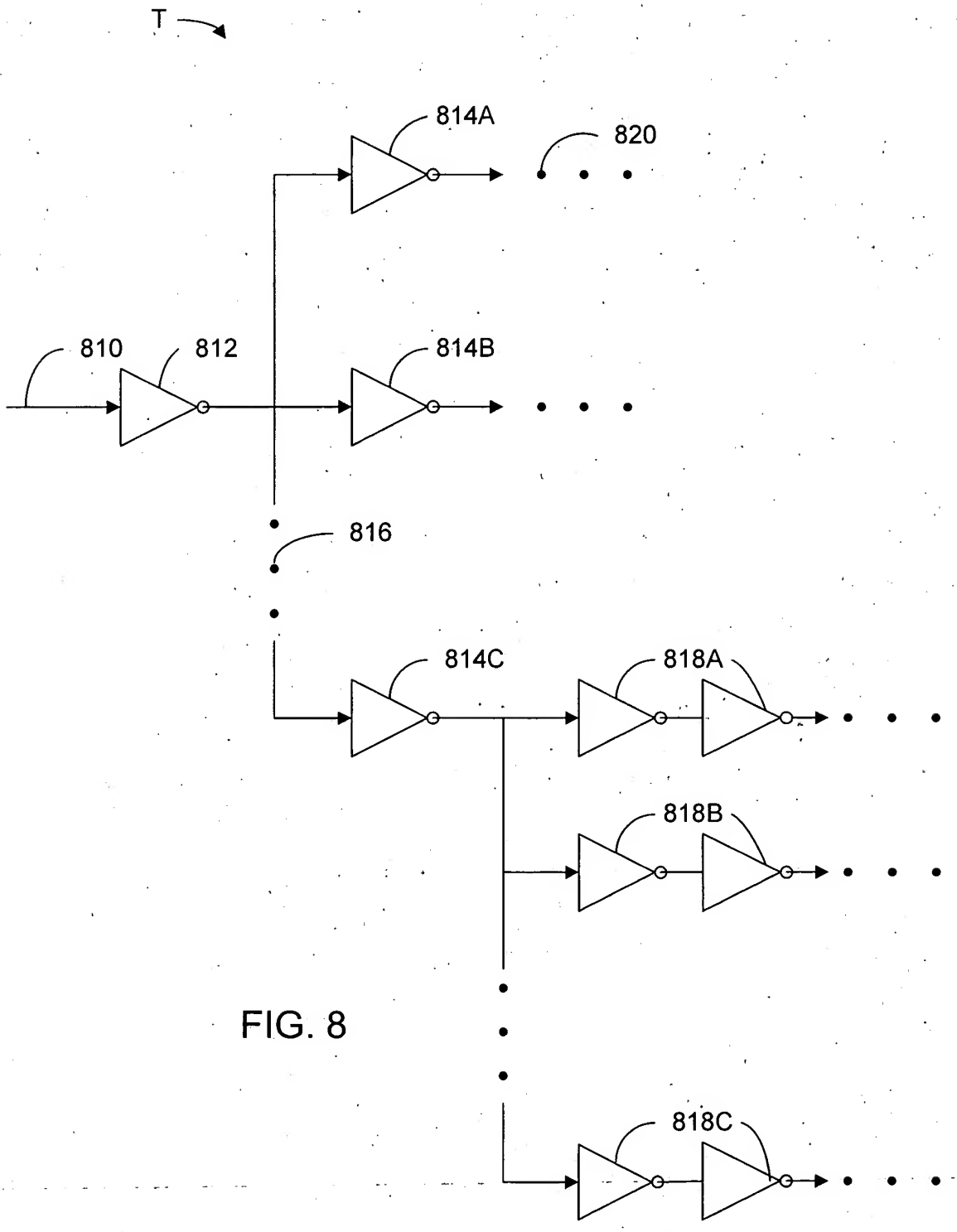

FIG. 8

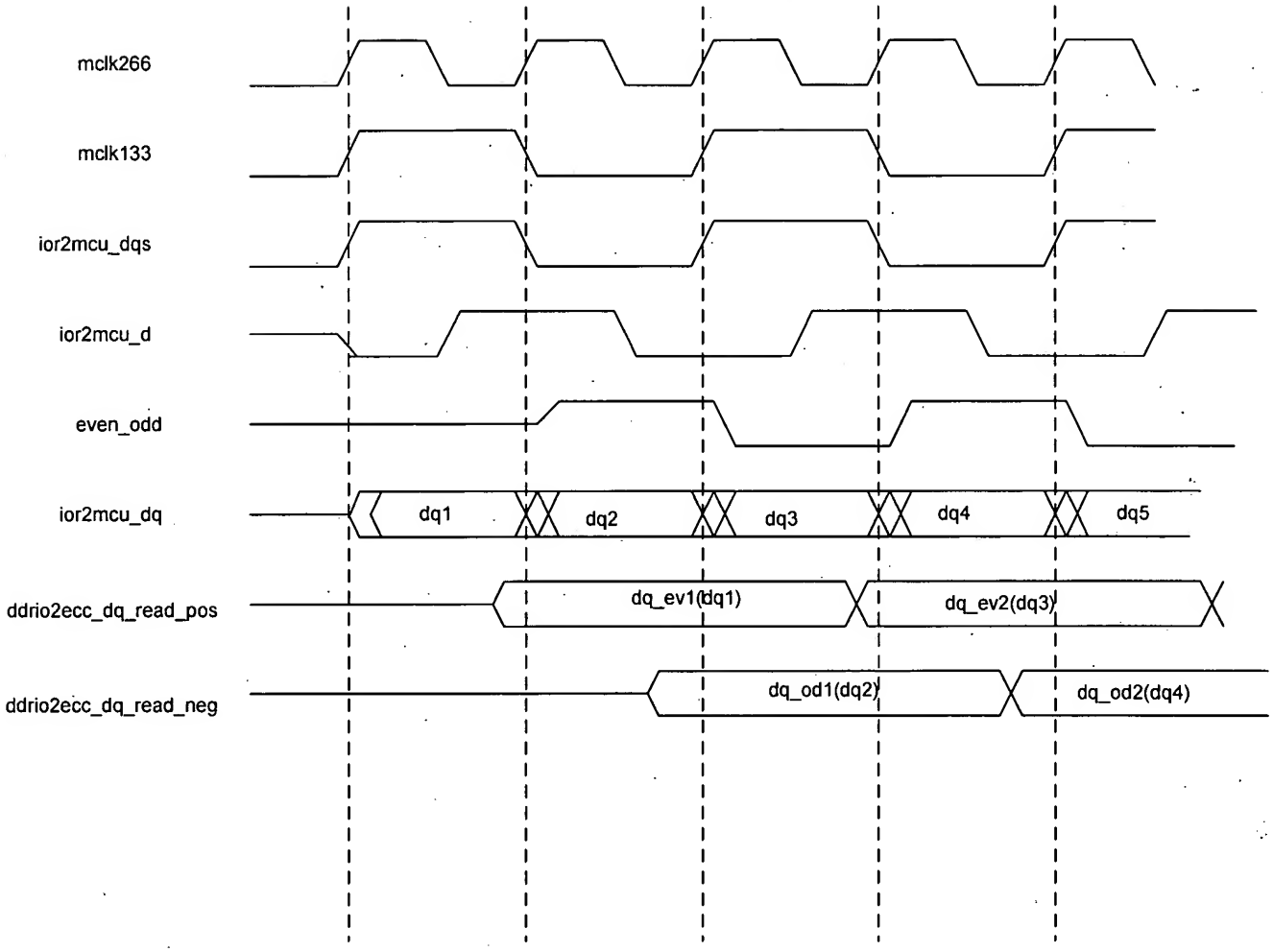
mclk266
mclk133
ior2mcu_dqs
ior2mcu_d
even_odd
ior2mcu_dq
dq1
dq2
dq3
dq4
dq5
ddrio2ecc_dq_read_pos
dq_ev1(dq1)
dq_ev2(dq3)
ddrio2ecc_dq_read_neg
dq_od1(dq2)
dq_od2(dq4)

FIG. 9

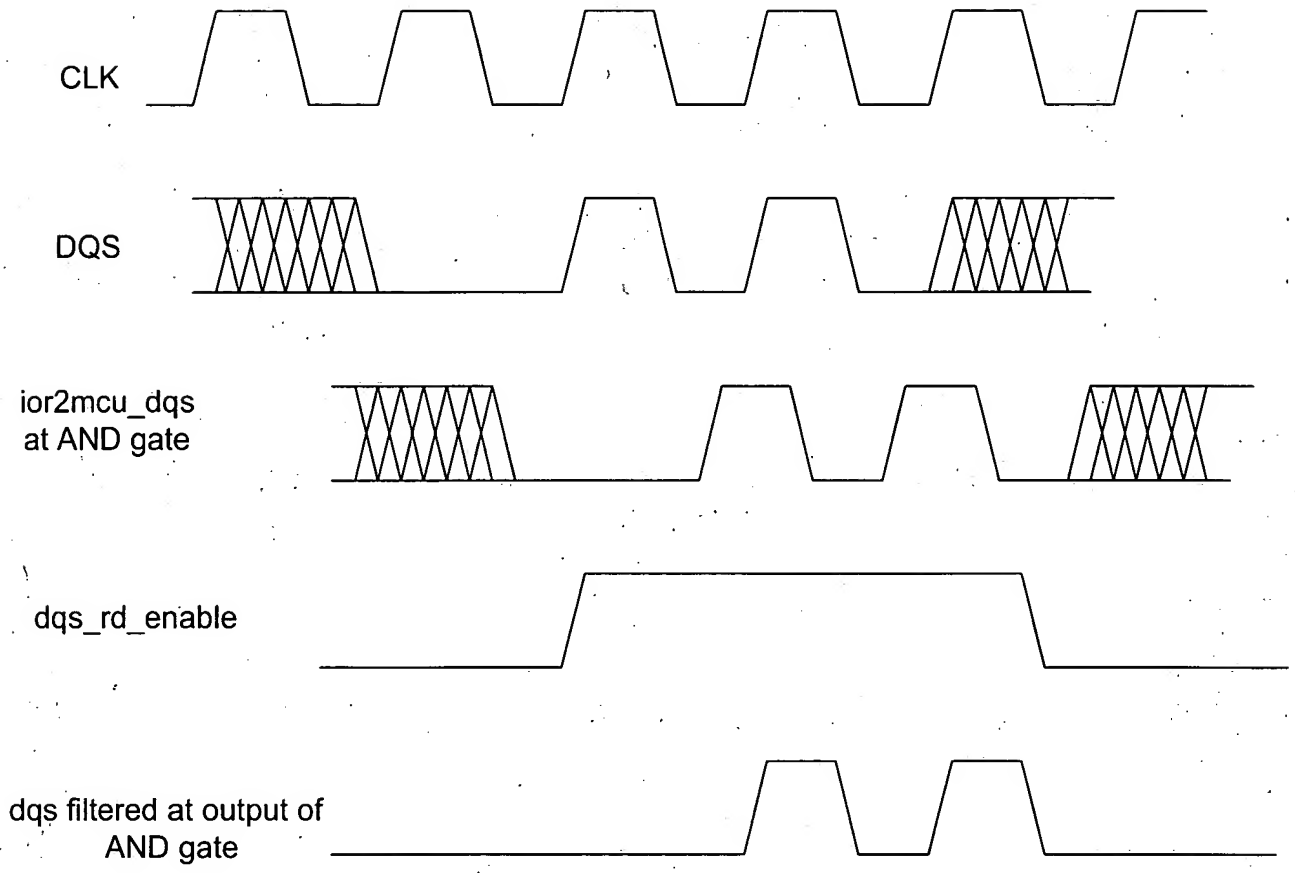
CLK
DQS
ior2mcu_dqs
at AND gate
dqs_rd_enable
dqs filtered at output of
AND gate

FIG. 10

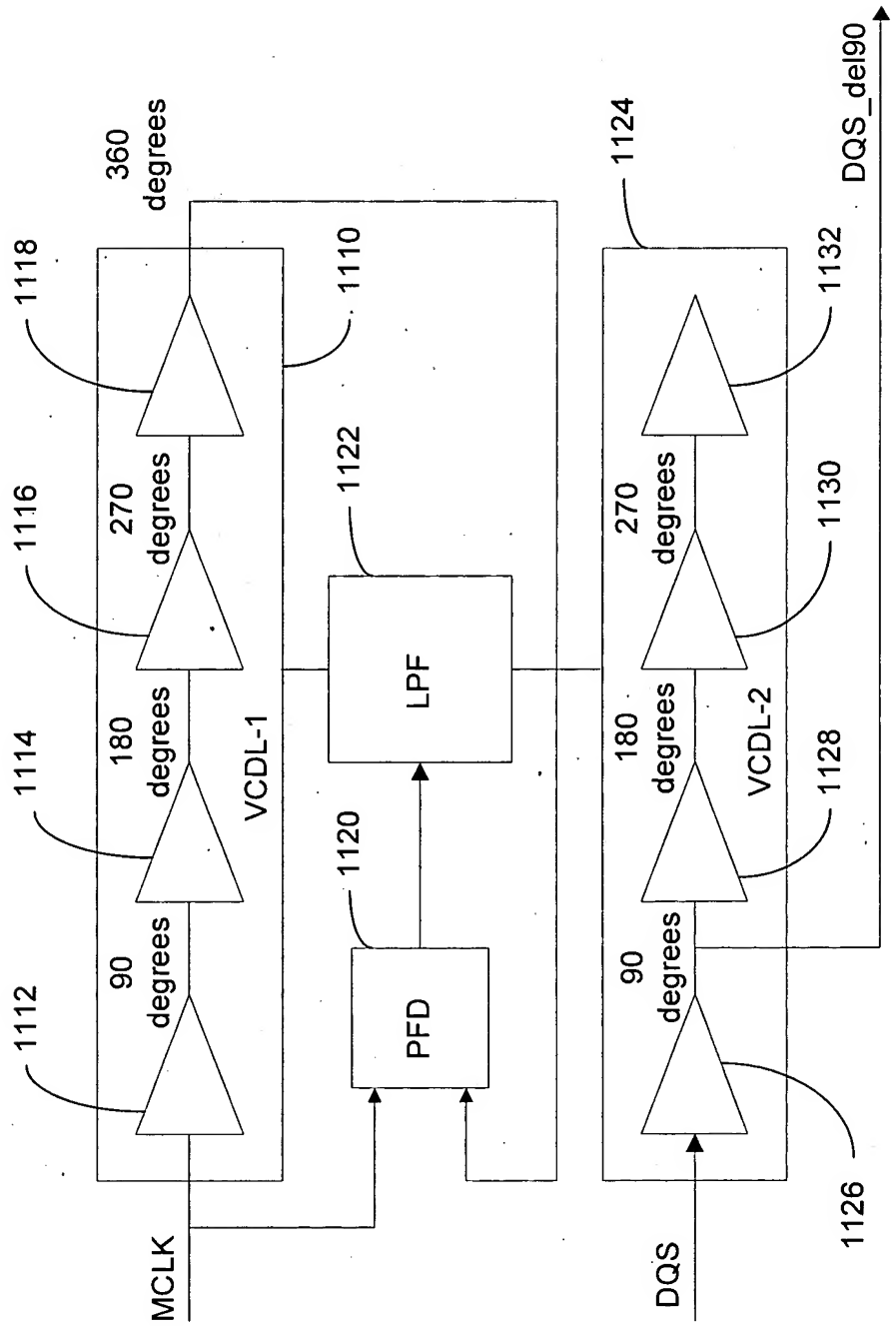
360 degrees
1118
1110
1124
DQS_del90
1132
270 degrees
1116
1122
270 degrees
1130
180 degrees
1114
VCDL-1
LPF
180 degrees
VCDL-2
1128
1120
90 degrees
1112
PFD
90 degrees
MCLK
DQS
1126

FIG. 11

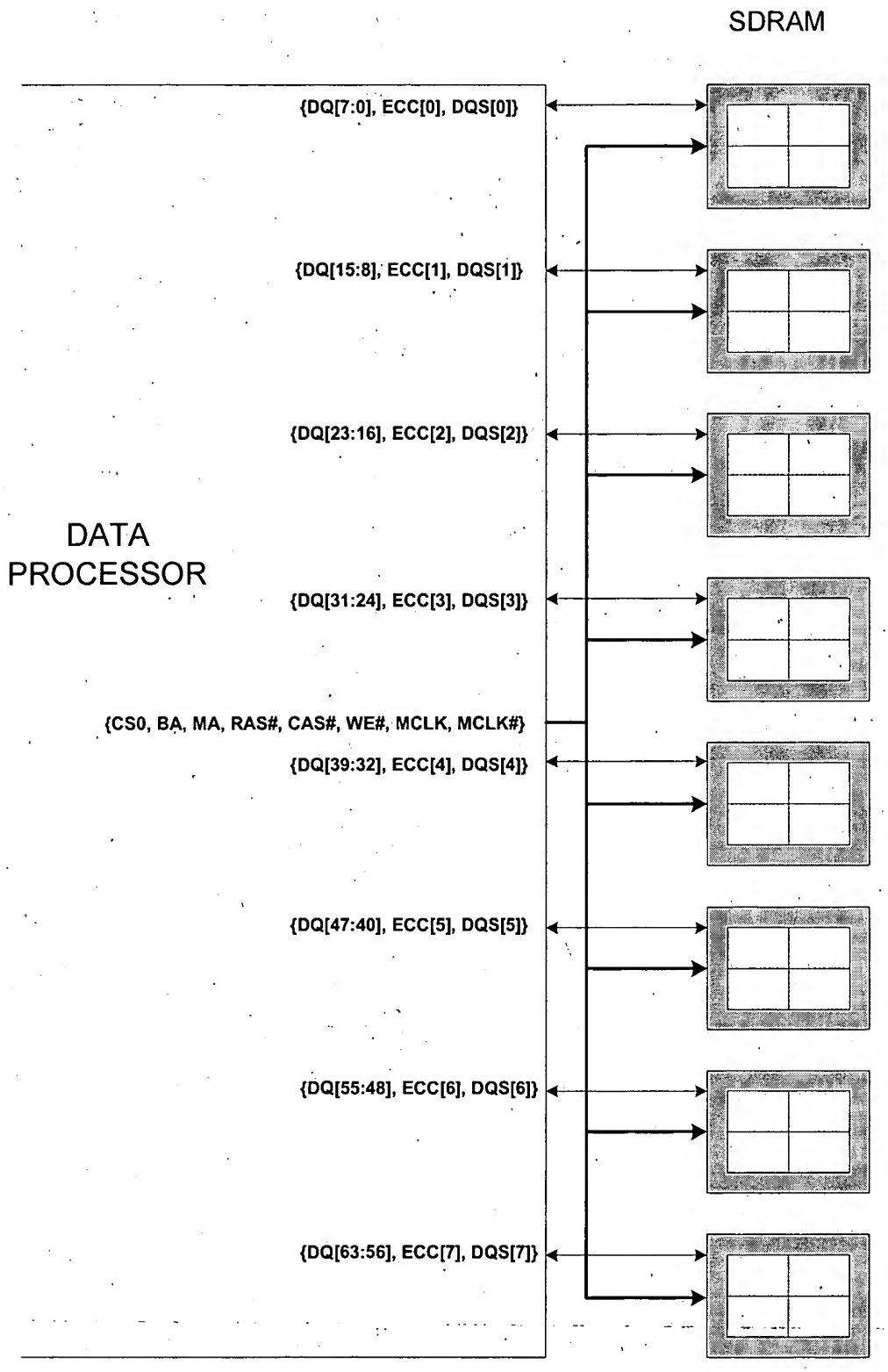
SDRAM
DATA PROCESSOR
{DQ[7:0], ECC[0], DQS[0]}
{DQ[15:8], ECC[1], DQS[1]}
{DQ[23:16], ECC[2], DQS[2]}
{DQ[31:24], ECC[3], DQS[3]}
{CS0, BA, MA, RAS#, CAS#, WE#, MCLK, MCLK#}
{DQ[39:32], ECC[4], DQS[4]}
{DQ[47:40], ECC[5], DQS[5]}
{DQ[55:48], ECC[6], DQS[6]}
{DQ[63:56], ECC[7], DQS[7]}

FIG. 12

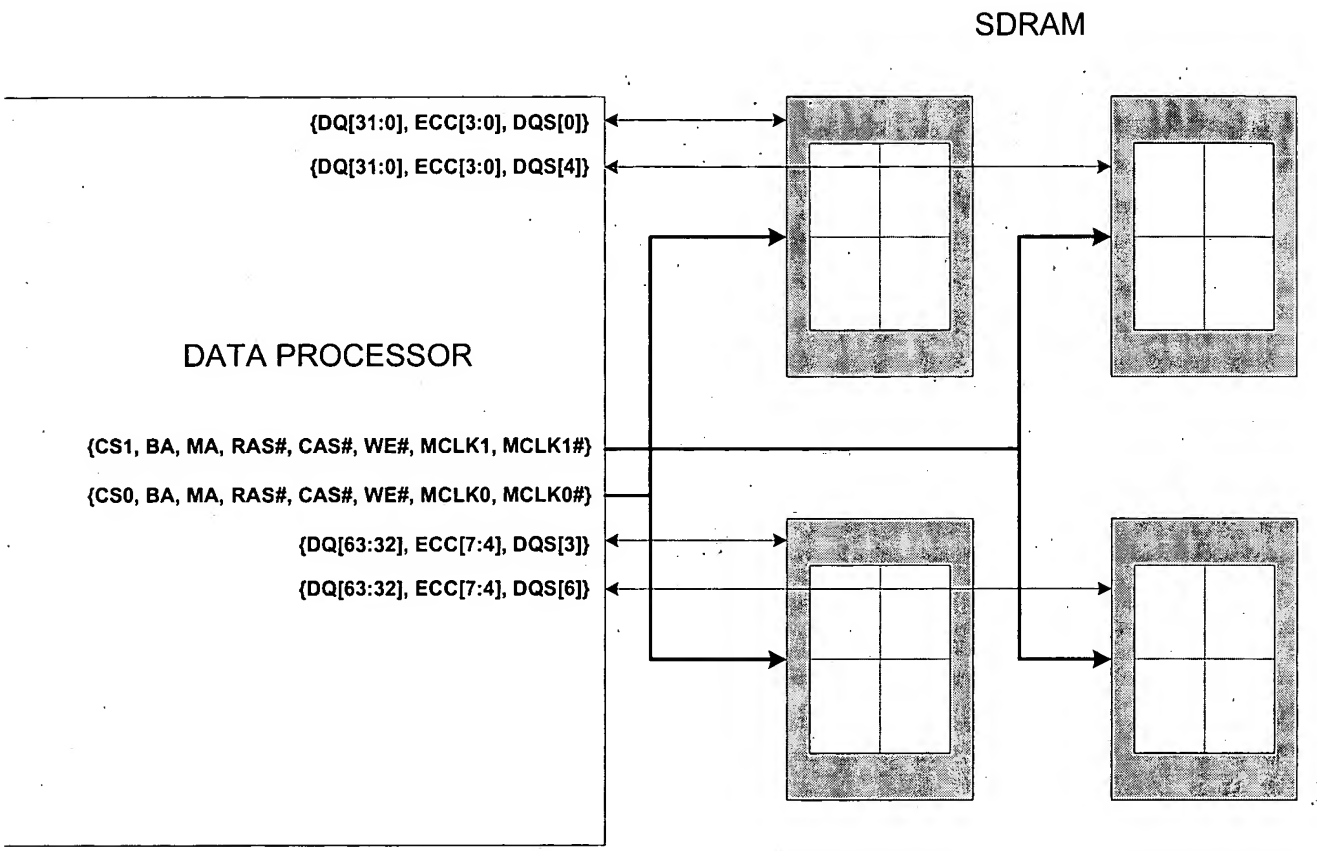
SDRAM
{DQ[31:0], ECC[3:0], DQS[0]}
{DQ[31:0], ECC[3:0], DQS[4]}
DATA PROCESSOR
{CS1, BA, MA, RAS#, CAS#, WE#, MCLK1, MCLK1#}
{CS0, BA, MA, RAS#, CAS#, WE#, MCLK0, MCLK0#}
{DQ[63:32], ECC[7:4], DQS[3]}
{DQ[63:32], ECC[7:4], DQS[6]}

FIG. 13